ABSTRACT

"Debugging of multiple data processors"

A router (2) in an integrated circuit (1) interfaces between a debug host (3) and a number N+1 of data processors (X10) and a TAP Controller (18). Data processor selection is dynamically in response to a SELX command from the debug host (3). Monitoring logic (19) determines length the combined data path and instruction/data memory fields of host commands, in order to extract the address which informs a multiplexer (15), which then synchronises signals accordingly. A switch multiplexer (16) bypasses the data processor multiplexer (15) for direct communication with control processors such as a TAP Controller (18).